		Application/Control No.	Applicant(s)/Patent Under Reexamination
Notice of References Cited		09/821,421	WILLIAMS ET AL.
		Examiner	Art Unit	
		Pierre-Michel Bataille	2186	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-6,578,117	06-2003	Weber, Wolf-Dietrich	711/151
*	B	US-6,415,369	07-2002	Chodnekar et al.	711/158
*	C	US-5,826,109	10-1998	Abramson et al.	711/151
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
*	U	Hardware Fault Containment in Scalable Shared-Memory Multiprocessors, D. Teodosiu et al., Computer Systems Laboratory, Stanford University (12 p.), 1977.
*	V	Johnson, Mike, "Superscalar Microprocessor Desighn", Englewood Cliffs, N.J.,: Prentice-hall, 1991, pp. vii-xi.
*	W	Rixner, Scott, Et Al., Memory Access Scheduling, To appear in ISCA-27 (2000), Computer Systems Laboratory, Stanford University, Stanford, CA 94305, pp. 1-11.
*	X	Direct Rambus (Technology Disclosure), "1.6 GM/memory sec", Oct. 1997, pp. 1-46.

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.